

## MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

2652/2652-1

R 28021

2652-1

## DESCRIPTION

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

## FEATURES

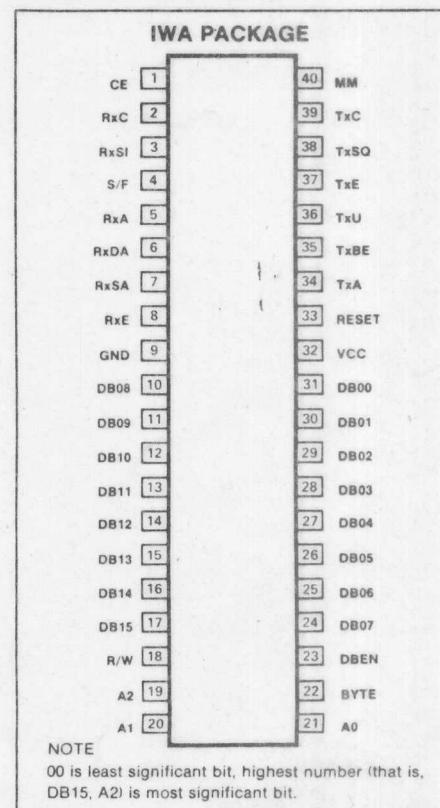
- DC to 1Mbps data rate, 2652-1 to 2Mbps
- Protocol management
  - Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
  - Byte-control protocols (BCP): BI-SYNC, DDCMP, limited BISYNC
- Programmable operation
  - 8 or 16-bit tri-state data bus
  - Protocol selection—BOP or BCP
  - Error control—CRC or VRC or no error check
  - Character length—1 to 8 bits for BOP or 5 to 8 bits for BCP
  - SYNC or secondary station address comparison for BCP-BOP
  - Idle transmission of SYNC/FLAG or MARK for BCP-BOP

- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character (will not overrun)
- SYNC generation, detection, and stripping for BCP
- Maintenance Mode for self-testing
- Common parameter control registers
- Independent status and data registers for receive and transmit
- Status indicator signals can be used as CPU interrupts
- TTL compatible
- 40-pin package
- Single +5V supply

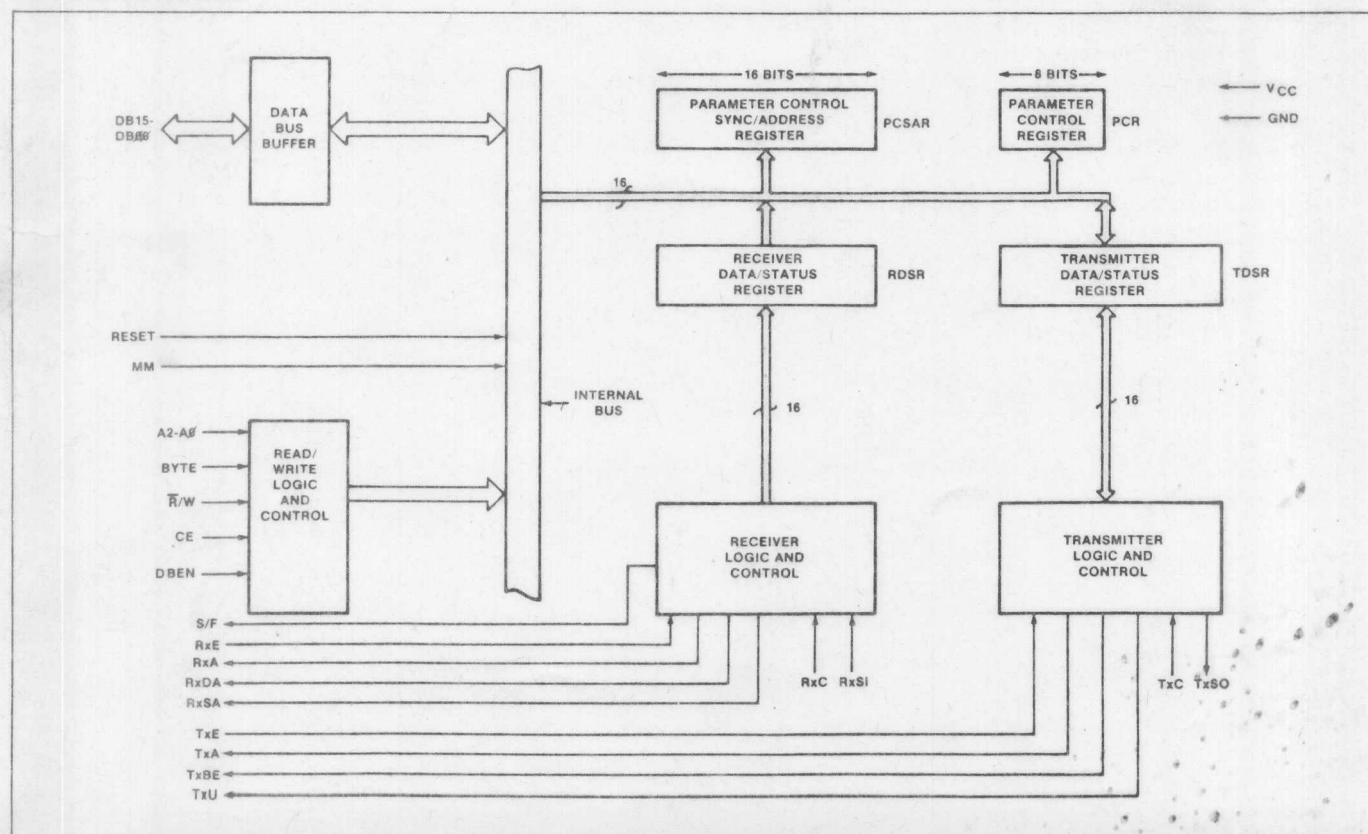
## APPLICATIONS

- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

### PIN CONFIGURATION



### BLOCK DIAGRAM



# signetics

## PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15-DB00	17-10 24-31	I/O	<b>Data Bus:</b> DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed onto an 8-bit data bus.
A2-A0	19-21	I	<b>Address Bus:</b> A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	<b>Byte:</b> Single byte (8 bit) data bus transfers are specified when this input is high. A low level specifies 16 bit data bus transfers.
CE	1	I	<b>Chip Enable:</b> A high input permits a data bus operation when DBEN is activated.
$\bar{R}/W$	18	I	<b>Read/Write:</b> $\bar{R}/W$ controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	<b>Data Bus Enable:</b> After A2-A0, CE, BYTE and $\bar{R}/W$ are set up, DBEN may be strobed. During a read, the tri-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	<b>Reset:</b> A high level initializes all internal registers (to zero) and timing.
MM	40	I	<b>Maintenance Mode:</b> MM internally gates TxSO back to RxSI and $\overline{TxC}$ to RxC for off line diagnostic purposes. The RxC input is disabled when MM is asserted.
RxE	8	I	<b>Receiver Enable:</b> A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	<b>Receiver Active:</b> RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC (PCSAR <sub>13</sub> ) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	<b>Receiver Data Available:</b> RxDA is asserted when an assembled character is in RDSRL and is ready to be presented to the processor. This output is reset when RDSRL is read.
RxC	2	I	<b>Receiver Clock:</b> RxC(1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	<b>SYNC/FLAG:</b> S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	<b>Receiver Status Available:</b> RxSA is asserted when there is a zero to one transition of any bit in RDSRH except for RSOM. It is cleared when RDSRH is read.
RxSI	3	I	<b>Receiver Serial Input:</b> RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	<b>Transmitter Enable:</b> A high level input enables the transmitter data path between TDSRL and TxSO. At the end of a message, a low level input causes TxSO = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	<b>Transmitter Active:</b> TxA is asserted when TxE is high and TSOM (TDSR <sub>8</sub> ) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	<b>Transmitter Buffer Empty:</b> TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	<b>Transmitter Underrun:</b> TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on PCSAR <sub>11</sub> . TxU is reset by RESET or setting of TSOM (TDSR <sub>8</sub> ). (TDSR <sub>8</sub> ).
TxC	39	I	<b>Transmitter Clock:</b> TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	<b>Transmitter Serial Output.</b> TxSO is the transmitted serial data. Mark = '1', space = '0'.
VCC	32	I	<b>+5V:</b> Power supply.
GND	9	I	<b>Ground:</b> 0V reference ground.

\*Indicates possible interrupt signal.

REGISTERS		NO. OF BITS	DESCRIPTION*
<b>Addressable</b>			
PCSAR	Parameter Control Sync/Address Register	16	PCSAR <sub>H</sub> and PCR contain parameters common to the receiver and transmitter. PCSAR <sub>L</sub> contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter Control Register	8	
RDSR	Receive Data/Status Register	16	RDSR <sub>H</sub> contains receiver status information. RDSR <sub>L</sub> = RxDB contains the received assembled character.
TDSR	Transmit Data/Status Register	16	TDSR <sub>H</sub> contains transmitter command and status information. TDSR <sub>L</sub> = TxDB contains the received assembled character.
<b>Internal</b>			
CCSR	Control Character Shift Register	8	These registers are used for character assembly (CCSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding Shift Register	16	
RxSR	Receiver Shift Register	8	
TxSR	Transmitter Shift Register	8	
RxCRC	Receiver CRC Accumulation Register	16	
TxCRC	Transmitter CRC Generation Register	16	

## NOTE

\*H = High byte - bits 15-8  
L = Low byte - bits 7-0

Table 1 GLOSSARY

CHARACTER	DESCRIPTION
FCS	Frame Check Sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ ) but can be otherwise determined by ECM. The inverted remainder is transmitted/received as the FCS with dividend preset to 1's.
BCC	Block Check Character is transmitted/received as two successive characters following the last data character of a BCP message. Usually CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ ) with dividend preset to 0's (as specified by ECM) is the polynomial. The CRC-16 is computed on all characters beginning with the first nonsync character at the start of the message.

Table 2 ERROR CONTROL

## FUNCTIONAL DESCRIPTION

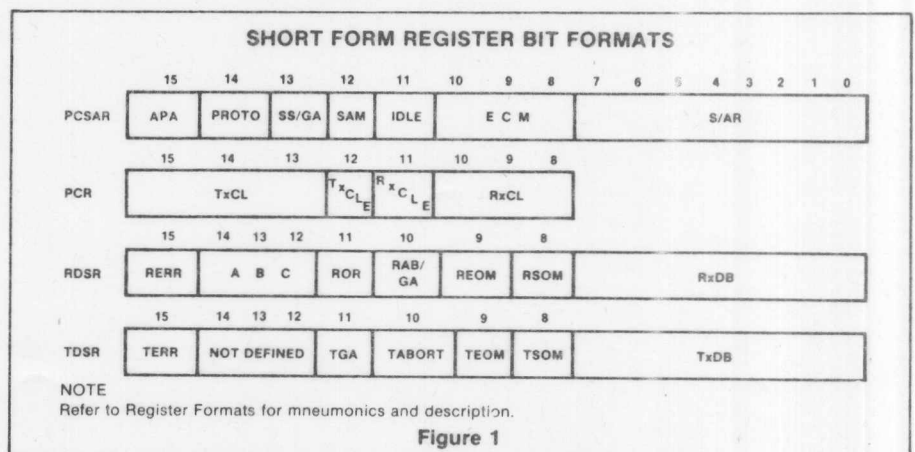
The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The MPCC block diagram is shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

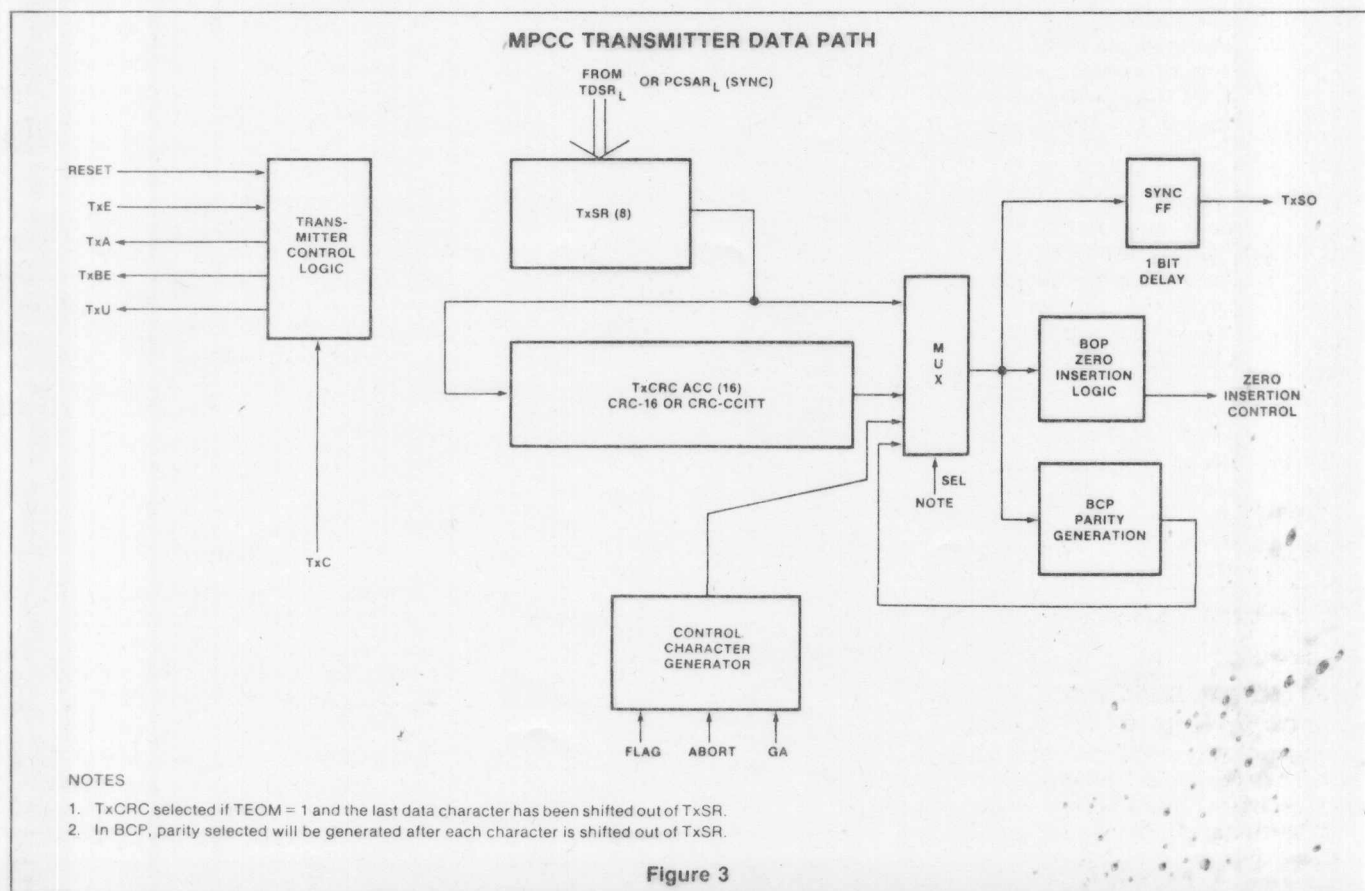
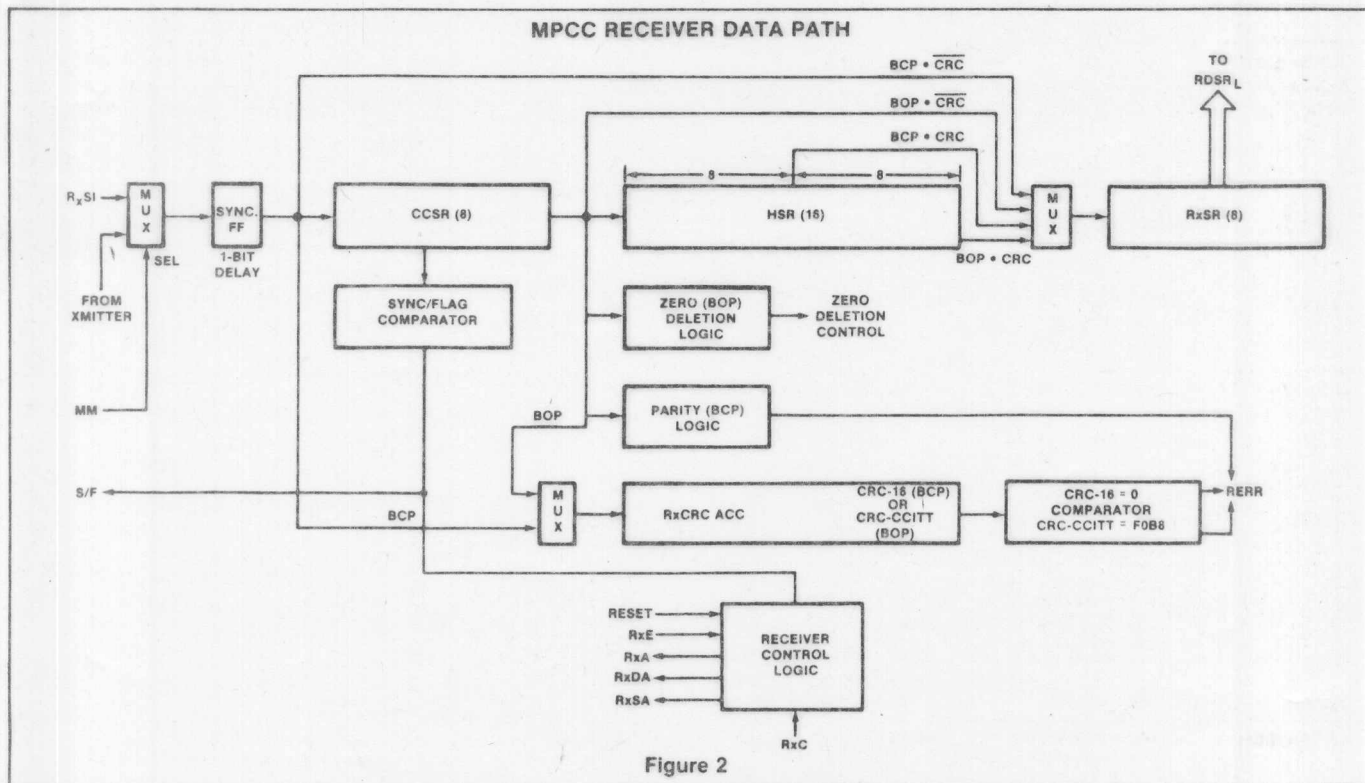
OPERATION	BIT PATTERN	FUNCTION
BOP	01111110	Frame message
FLAG	11111111 generation	Terminate communication
ABORT	01111111 detection	
GA	01111111	Terminate loop mode repeater function
Address	(PCSAR <sub>L</sub> ) <sup>1</sup>	Secondary station address
BCP		
SYNC	(PCSAR <sub>L</sub> ) or (TxDB) <sup>2</sup> generation	Frame message

## NOTES

1. ( ) refers to contents of
2. For IDLE = 0 or 1 respectively

Table 3 SPECIAL CHARACTERS





## RECEIVER OPERATION

## General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

## BOP Operation

A flow chart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the RDSR<sub>L</sub> for presentation to the processor. At that time the RxD<sub>A</sub> output will be asserted and the processor must take the character before the next character is assembled in the RxSR. If not, an overrun (RDSR<sub>11</sub> = 1) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ( $\text{PCSAR}_{12} = 1$ ), the contents of  $\text{RxsR}$  are compared with the address stored in  $\text{PCSAR}_L$ . A match indicates the forthcoming message is intended for the station; the  $\text{RxA}$  output is asserted, the character is loaded into  $\text{RDSR}_L$ ,  $\text{RxDa}$  is asserted and the Receive Start of Message bit ( $\text{RSOM}$ ) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is a primary station ( $PCRSAR_{12} = 0$ ), no secondary address check is made;  $RxA$  is asserted and  $RSOM$  is set once the first non-FLAG character has been loaded into  $RDSR_L$  and  $RxDa$  has been asserted. Extended address field can be supported by software if  $PCRSAR_{12} = 0$ .

When the 8 bits following the address character have been loaded into RDSRL and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the Information field by the processor. It will be assembled into character lengths as specified by PCR<sub>8-10</sub>. As before, RxDA is asserted each time a char-

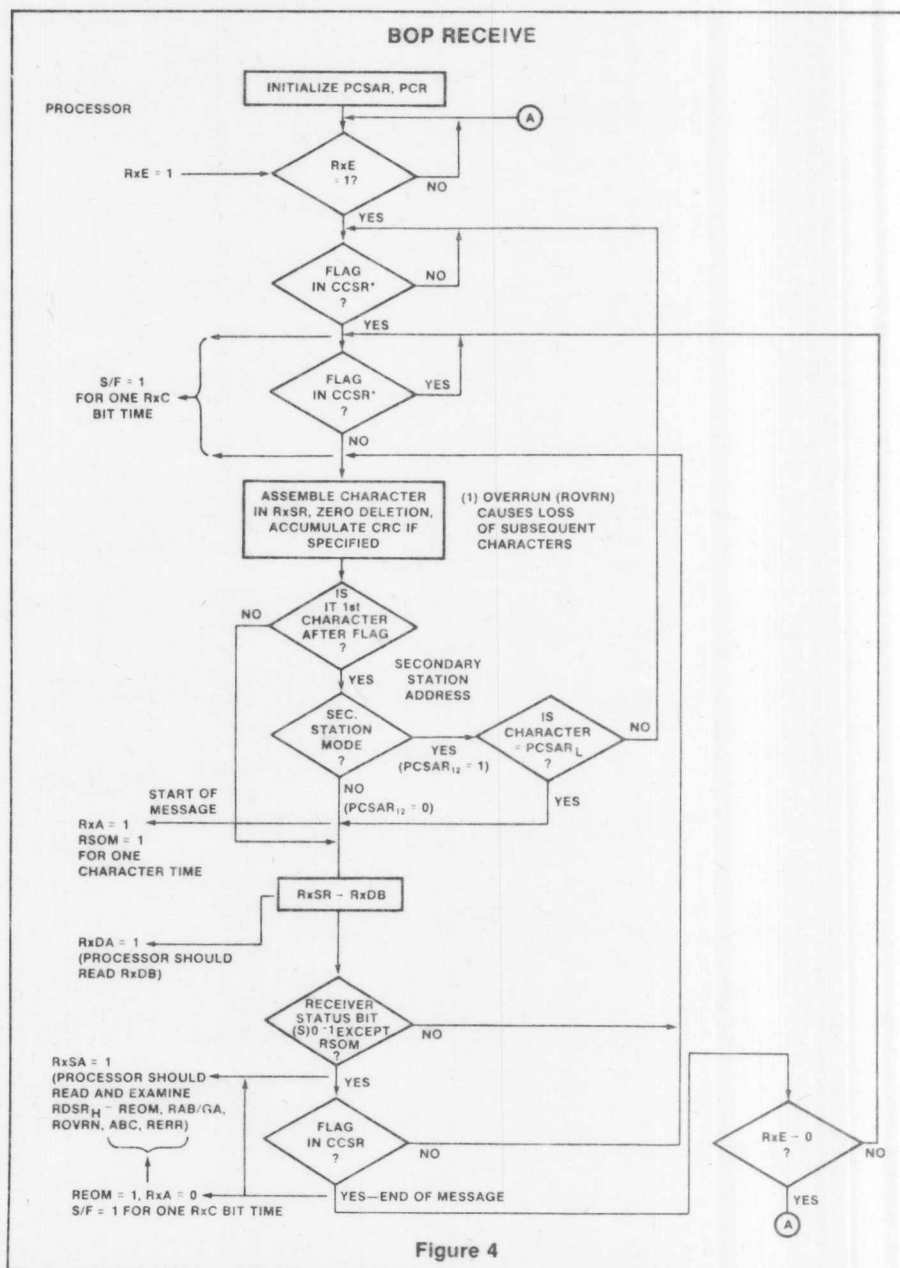


Figure 4

acter has been transferred into RDSR<sub>L</sub> and is cleared when RDSR<sub>L</sub> is read by the processor. RDSR<sub>H</sub> should only be read when RxSA is asserted. This occurs on a zero to one transition of any bit in RDSR<sub>H</sub> except for RSOM. RxSA and all bits in RDSR<sub>H</sub> except RSOM are cleared when RDSR<sub>H</sub> is read. The processor should check RDSR<sub>9-15</sub> each time RxSA is asserted. If RDSR<sub>9</sub> is set, then RDSR<sub>12-15</sub> should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next receiver

character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e. there will not be an overrun.

The CRC-CCITT, if specified by PCSAR<sub>8-10</sub>, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in RDSR<sub>L</sub> and the receiver status in RDSR<sub>9-15</sub>. If RDSR<sub>15</sub> = 1, there has been a

transmission error; the accumulated CRC-CCITT is incorrect. If  $RDSR_{12-14} \neq 0$ , the last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

### BCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by  $PCR_{8-10}$ , that match the contents of  $PCSAR_L$ . The next non-SYNC character or next SYNC character if stripping is not specified ( $PCSAR_{13} = 0$ ), causes RxA to be asserted and enables the receiver data path from CCSR through  $HSR_L$  to  $RxSR$ . All characters following the first non-SYNC are assembled in  $RxSR$  and loaded into  $RDSR_L$ . RxDA is active when a character is available in  $RDSR_L$ . RxSA is active on a 0 to 1 transition of any bit in  $RDSR_H$ . The signals are cleared when  $RDSR_L$  or  $RDSR_H$  are read respectively.

If CRC-16 error control is specified by  $PCSAR_{8-10}$ , the processor must determine the last character received prior to the CRC field. When that character is loaded into  $RDSR_L$  and RxDA is asserted, the received CRC will be in CCSR and  $HSR_L$ . To check for a transmission error, the processor must read the receiver status ( $RDSR_H$ ) and examine  $RDSR_{15}$ . This bit will be set for one character time if an error free message has been received. If  $RDSR_{15} = 0$ , the CRC-16 is in error. Note that this bit should be examined only at the end of a message and that the accumulated CRC will include all characters starting with the first non-SYNC character at the start of the message. In particular, SYNC's in the middle of a message, DLE characters, and the first SOH or STX after line turn around are subject to CRC. This necessitates external CRC generation/checking when supporting IBM's BISYNC.

If VRC had been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes  $RDSR_{15}$  to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor. The processor should compute and check LRC if required.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

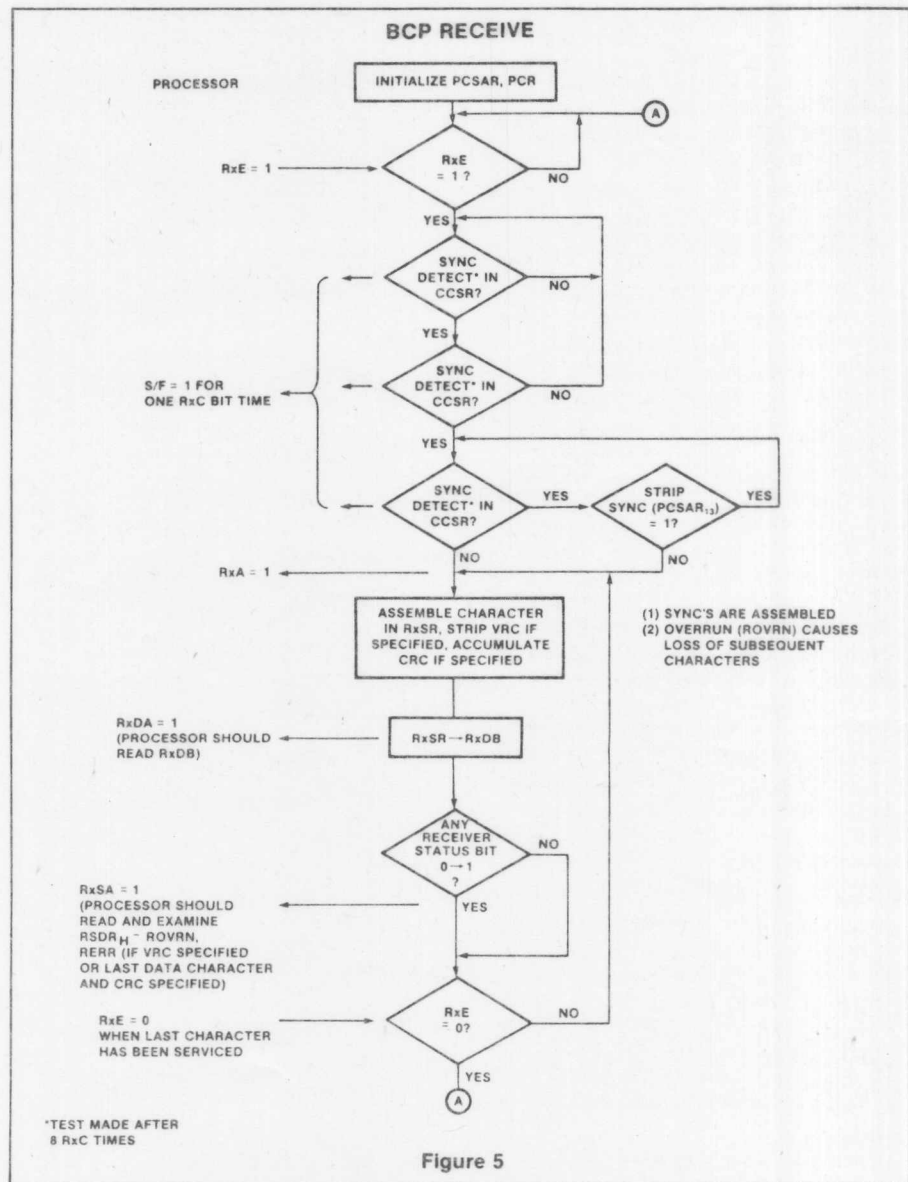


Figure 5

### TRANSMITTER OPERATION

#### General

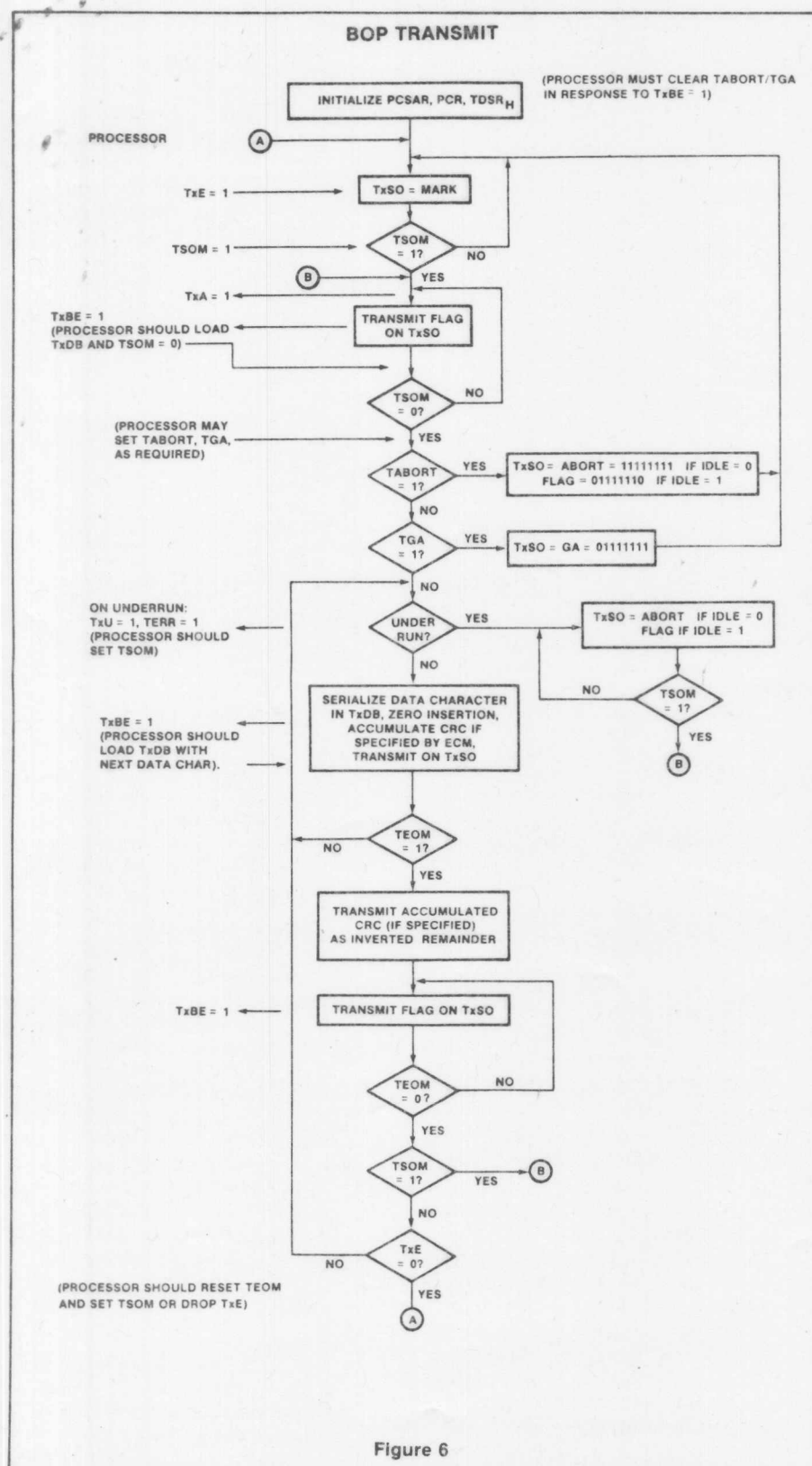
After the parameter control register (PCSAR and PCR) have been initialized, Tx E must be set high to enable the transmitter data path. TxSO is held to mark until TSOM ( $TDSR_0$ ) is set. Then, transmitter operation depends on protocol mode.

#### BOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent when the processor sets the Transmit Start of Message bit (TSOM). The FLAG is used to synchronize the message that follows. Tx A will be asserted after TSOM is set. When TxBE is asserted by the MPCC, the processor should load

$TDSR_L$  with the first character of the message. TSOM should be cleared at the same time  $TDSR_L$  is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGs are sent as long as TSOM  $\neq 1$ .

All succeeding characters are loaded into  $TDSR_L$  by the processor when TxBE = 1. Each character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode ( $PCSAR_{8-10}$ ). The FCS should be the



CRC-CCITT polynomial)  $X^{16} + X^{12} + X^5 + 1$ ) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR (TDSR<sub>15</sub>) will be asserted with ABORT or FLAG used as the TxSQ line fill depending on the state of IDLE (PCSA<sub>R11</sub>). The processor must set TSOM to reset the underrun condition. To retransmit the message the processor should proceed with the normal start of message sequence.

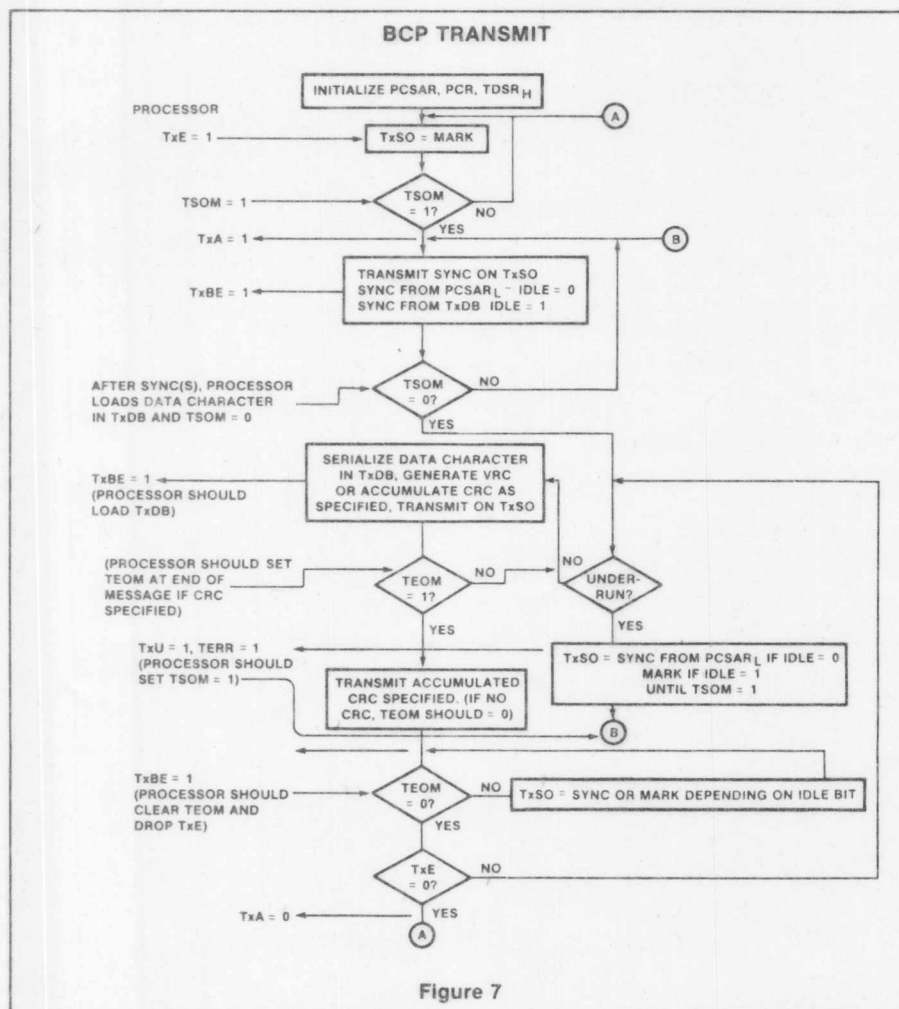
A residual character of 1 to 7 bits may be transmitted at the end of the Information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into TDSR<sub>L</sub> and sent to TxSR (TxBE = 1), the processor should set TEOM (TDSR<sub>9</sub>). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop Tx<sub>E</sub> when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When Tx<sub>E</sub> has been dropped, Tx<sub>A</sub> will be low 1 1/2 bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading TDSRL with a data character and then simply resetting TEOM (without setting TSOM).

### BCP Operation

Transmitter operation for BCP mode is shown in Figure 7. If TxE is high, TxA will be asserted when TSOM = 1. At that time SYNC characters are sent from PCSAR<sub>L</sub> or TDSR (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For more than one SYNC, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from TDSR<sub>L</sub>, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the TxSO line fill depend on IDLE (PCSAR<sub>11</sub>). The processor must set TSOM and retransmit the message to recover. This is not compatible with IBM's BISYNC, so that the user must not underrun when supporting that protocol.



CRC-16, if specified by PCSAR<sub>8-10</sub>, is generated on each character transmitted from TDSR<sub>L</sub> when TSOM = 0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data character and the CRC-16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC-16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC-16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TxE and TSOM.

If LRC is required, it must be generated by the processor and transmitted after the last data character. TEOM should not be set under this condition. If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC TEOM should be set only if SYNCs are required at the end of the message block.

### SPECIAL CASE

The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

### PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC-CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.

### DATA BUS CONTROL

The processor must set up the MPCC register address (A2-A0), chip enable (CE), byte select (BYTE), and read/write (R/W) inputs before each data bus transfer operation.

During a read operation (R/W = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15-08 or DB07-00 depending on the H/L status of the register addressed. Unused bits in RDSR<sub>L</sub> are zero. If BYTE = 0, all 16 bits (DB15-00) contain MPCC information. The trailing edge of DBEN will reset RxD<sub>A</sub> and/or RxD<sub>S</sub> if RDSR<sub>H</sub> or RDSR<sub>L</sub> is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation (R/W = 1), data must be stable on DB15-08 and/or DB07-00 prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was TDSR<sub>H</sub> or TDSR<sub>L</sub>.

	A2	A1	A0	REGISTER
<b>BYTE = 0</b>	<b>16-BIT DATA BUS = DB<sub>15</sub> - DB<sub>00</sub></b>			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
<b>BYTE = 1</b>	<b>8-BIT DATA BUS = DB<sub>7-0</sub> or DB<sub>15-8</sub>**</b>			
	0	0	0	RDSR <sub>L</sub>
	0	0	1	RDSR <sub>H</sub>
	0	1	0	TDSR <sub>L</sub>
	0	1	1	TDSR <sub>H</sub>
	1	0	0	PCSAR <sub>L</sub>
	1	0	1	PCSAR <sub>H</sub>
	1	1	0	PCR <sub>L</sub> *
	1	1	1	PCR <sub>H</sub>

## NOTES

\* PCR lower byte does not exist. It will be all "0"s when read.

\*\* Corresponding high and low order pins should be tied together.

Table 4 MPCC REGISTER ADDRESSING

BIT	NAME	MODE	FUNCTION																																				
00-07	Not Defined																																						
08-10	RxCL	BOP/BCP	<p>Receiver Character Length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received.</p> <table> <tr> <th>10</th><th>9</th><th>8</th><th>Char. length (bits)</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>8</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>2</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>3</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>4</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>5</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>6</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>7</td></tr> </table>	10	9	8	Char. length (bits)	0	0	0	8	0	0	1	1	0	1	0	2	0	1	1	3	1	0	0	4	1	0	1	5	1	1	0	6	1	1	1	7
10	9	8	Char. length (bits)																																				
0	0	0	8																																				
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0	1	0	2																																				
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1	0	1	5																																				
1	1	0	6																																				
1	1	1	7																																				
11	RxCLE	BOP/BCP	Receiver Character Length Enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading.																																				
12	TxCLE	BOP/BCP	Transmitter Character Length Enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading.																																				
13-15	TxCL	BOP/BCP	Transmitter Character Length is loaded by the processor when TxCLE = 0. Character bit length specification format is identical to RxCL. It is valid after transmission of single byte address and control fields.																																				

Table 5 PARAMETER CONTROL REGISTER (PCR)-(R/W)

BIT	NAME	MODE	FUNCTION					
00-07	S/AR	BOP	SYNC/ADDRESS Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station. SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.					
		BCP						
08-10	ECM	BOP/BCP	<b>Error Control Mode</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>Suggested Mode</b>	<b>Char. length</b>
			CRC-CCITT preset to 1's	0	0	0	BOP	1-8
			CRC-CCITT preset to 0's	0	0	1	BOP	1-8
			Not used	0	1	0	---	
			CRC-16 preset to 0's	0	1	1	BCP	8
			VRC odd	1	0	0	BCP	5-7
			VRC even	1	0	1	BCP	5-7
			Not used	1	1	0	---	
			No error control	1	1	1	BCP/BOP	5-8
			ECM should be loaded by the processor during initialization or when both data paths are idle.					
			11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.		
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1.					
		BCP	IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.					
			IDLE = 0 transmit initial SYNC characters and underrun line fill characters from the S/AR.					
			IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.					
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.					
13	SS/GA	BOP	Strip SYNC/Go Ahead. Operation depends on mode. For loop mode only SS/GA = 1 enables GA detection following a closing FLAG. When a GA is detected REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 causes the receiver to be disabled upon detection of an ABORT, GA, or FLAG.					
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.					
14	PROTO	BOP BCP	Determines MPCC Protocol mode PROTO = 0 BOP PROTO = 1 BCP					
15	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.					

Table 6 PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	TxDB	BOP/BCP	Transmit Data Buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM	BOP BCP	<p>Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1.</p> <p>TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation begins. FCS, as specified by PCSAR<sub>8-10</sub>, should be CRC-CCITT preset to 1's.</p> <p>TSOM = 1 generates SYNCs from PCSAR<sub>L</sub> or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.</p>

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15)

BIT	NAME	MODE	FUNCTION
09	TEOM	BOP	Transmit End of Message. Used to terminate a transmitted message when CRC error checking is used. TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGS are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from PCSAR <sub>L</sub> or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter Abort = 1 will cause ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12-14	Not Defined		
15	TERR	Read only  BOP BCP	Transmitter Error = 1 indicates the TxDB has not been loaded in time (one character time - 1/2 Tx period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1) SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15) (Cont'd)

BIT	NAME	MODE	FUNCTION
00-07	RxDB	BOP/BCP	Receiver Data Buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
09	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading RDSR <sub>H</sub> , reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading RDSR <sub>H</sub> , reset operation, or dropping of RxE. A received ABORT inhibits RxDA.
11	ROR	BOP/BCP	Receiver Overrun = 1 indicates the processor has not read last character in the RxDB within one character time + 1/2 Rx period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading RDSR <sub>H</sub> , reset operation, or dropping of RxE.
12-14	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by PCSCR <sub>8-10</sub> . Otherwise, ABC = number of bits in the last data character. ABC is cleared when RDSR <sub>H</sub> is read, reset operation, or dropping RxE. The residual character is right justified in RDSR <sub>L</sub> .
15	RERR	BOP  BCP	Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC-CCITT preset to 1's should be specified by PCSAR <sub>8-10</sub> : RERR = 1 indicates FCS error (CRC ≠ F0B8) RERR = 0 indicates FCS received correctly (CRC = F0B8) CRC-16 preset to 0's on 8-bit data characters specified by PCSAR <sub>8-10</sub> : RERR = 1 indicates CRC-16 received correctly (CRC = 0). RERR = 0 indicates CRC-16 error (CRC ≠ 0) VRC specified by PCSAR <sub>8-10</sub> : RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct

Table 8 RECEIVER DATA/STATUS REGISTER (RDSR)-(Read Only)

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

PARAMETER	RATING	UNIT
T <sub>A</sub> Operating ambient temperature <sup>2</sup>	0 to +70	°C
T <sub>STG</sub> Storage temperature	-65 to +150	°C
Input or output voltages with respect to GND <sup>3</sup>	-0.3 to +15	V
V <sub>CC</sub> With respect to GND	-0.3 to +7	V

DC ELECTRICAL CHARACTERISTICS T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5V ± 5%<sup>4,5,6</sup>

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V <sub>IL</sub> Input voltage Low				0.8	V
V <sub>IH</sub> Input voltage High		2.0			
V <sub>OL</sub> Output voltage Low	I <sub>OL</sub> = 1.6mA			0.4	V
V <sub>OH</sub> Output voltage High	I <sub>OH</sub> = -100μA	2.4			
I <sub>CC</sub> Power supply current	V <sub>CC</sub> = 5.25V, T <sub>A</sub> = 0°C			150	mA
I <sub>IL</sub> Leakage current Input	V <sub>IN</sub> = 0 to 5.25V			10	μA
I <sub>OL</sub> Leakage current Output	V <sub>OUT</sub> = 0 to 5.25V			10	
C <sub>IN</sub> Capacitance Input	V <sub>IN</sub> = 0V, f = 1MHz			20	pF
C <sub>OUT</sub> Capacitance Output	V <sub>OUT</sub> = 0V, f = 1MHz			20	

AC ELECTRICAL CHARACTERISTICS T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V ± 5%, AC timing indicated is with outputs unloaded.<sup>4,5,6</sup>

PARAMETER	2652			2652-1			UNIT
	Min	Typ	Max	Min	Typ	Max	
t <sub>ACS</sub> Setup and hold time	50			50			ns
t <sub>ACH</sub> Address/control setup	0			0			
t <sub>DS</sub> Address/control hold	50			50			
t <sub>DH</sub> Data bus setup (write)	0			0			
t <sub>RXS</sub> Data bus hold (write)	150			150			
t <sub>RxH</sub> Receiver serial data transfer	150			150			
t <sub>RES</sub> Receive serial data hold							
t <sub>RES</sub> Pulse width	250			250			ns
t <sub>DBEN</sub> RESET	250			250			
t <sub>DD</sub> DBEN							
t <sub>DD</sub> Delay time			200			200	ns
t <sub>TXD</sub> Data bus (read)			400			400	
t <sub>DF</sub> Transmit serial data			150			150	ns
f			1.0			2.0	MHz
t <sub>CLK1</sub> Data bus float time (read)	500			250			ns
t <sub>CLK0</sub> Clock high	500			250			ns

m = minimum value of {RxC low, RxC high, TxC low, TxC High}

## NOTES

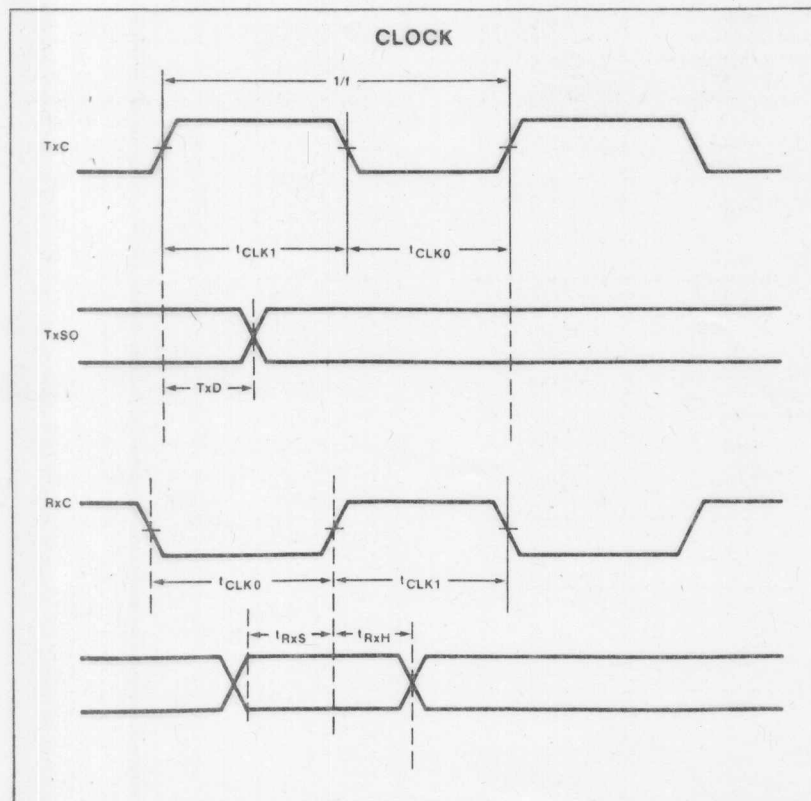
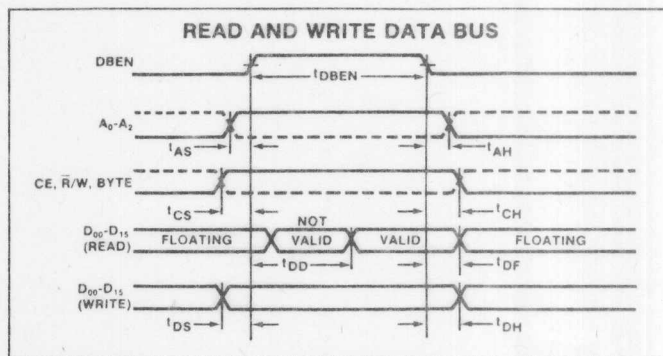
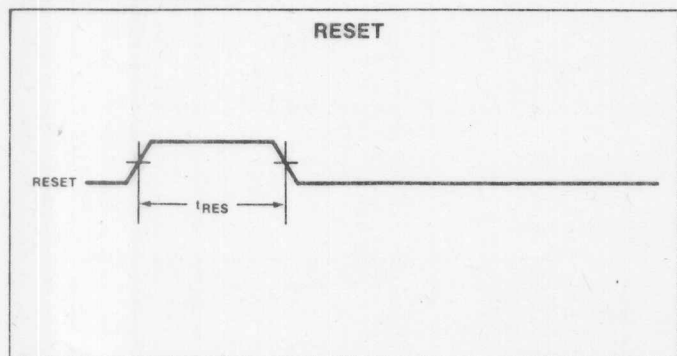
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60° C/W junction to ambient (IQ ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. All time measurements are at the  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ , or  $V_{IL}$  levels as appropriate.
6. Min/max values are at +25°C, nominal supply voltages, and nominal processing parameters.

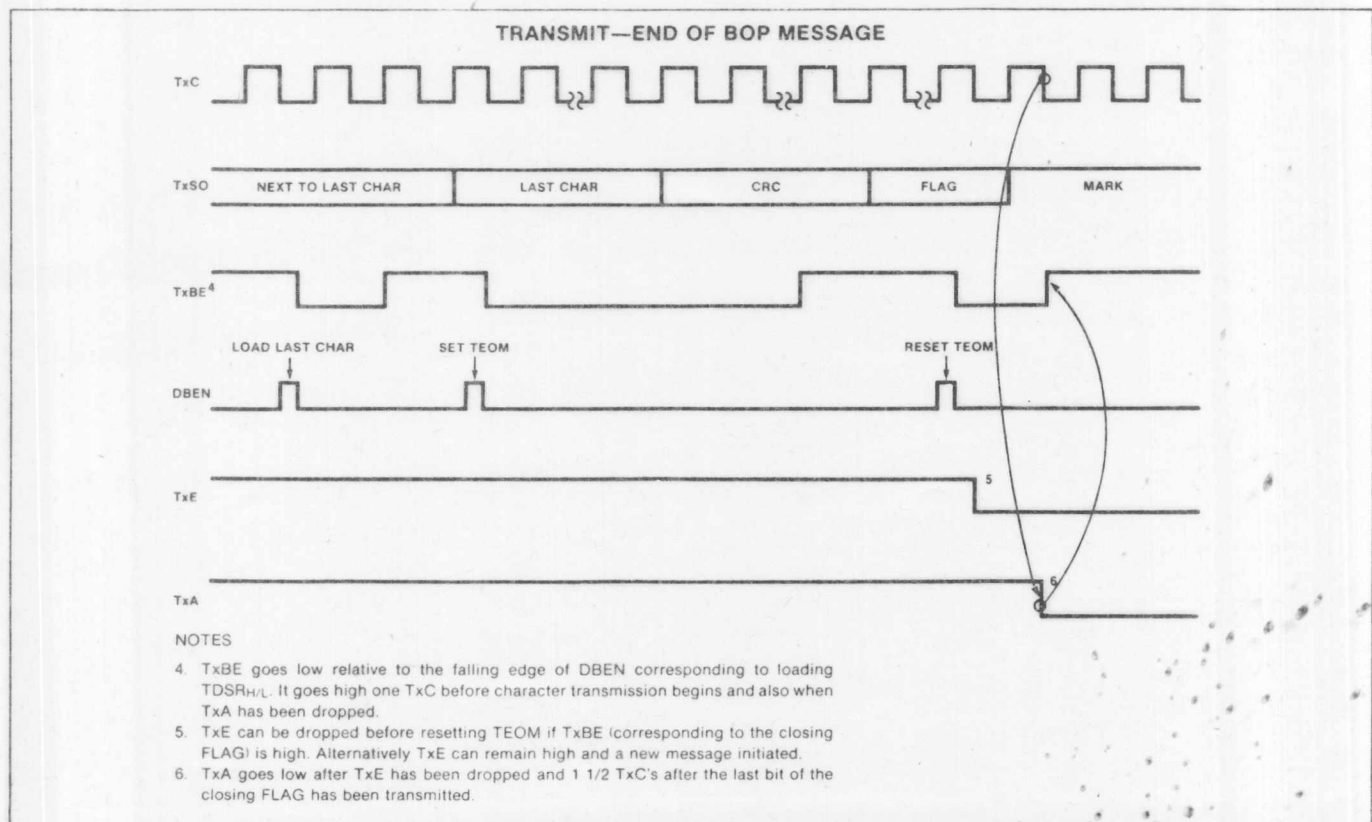
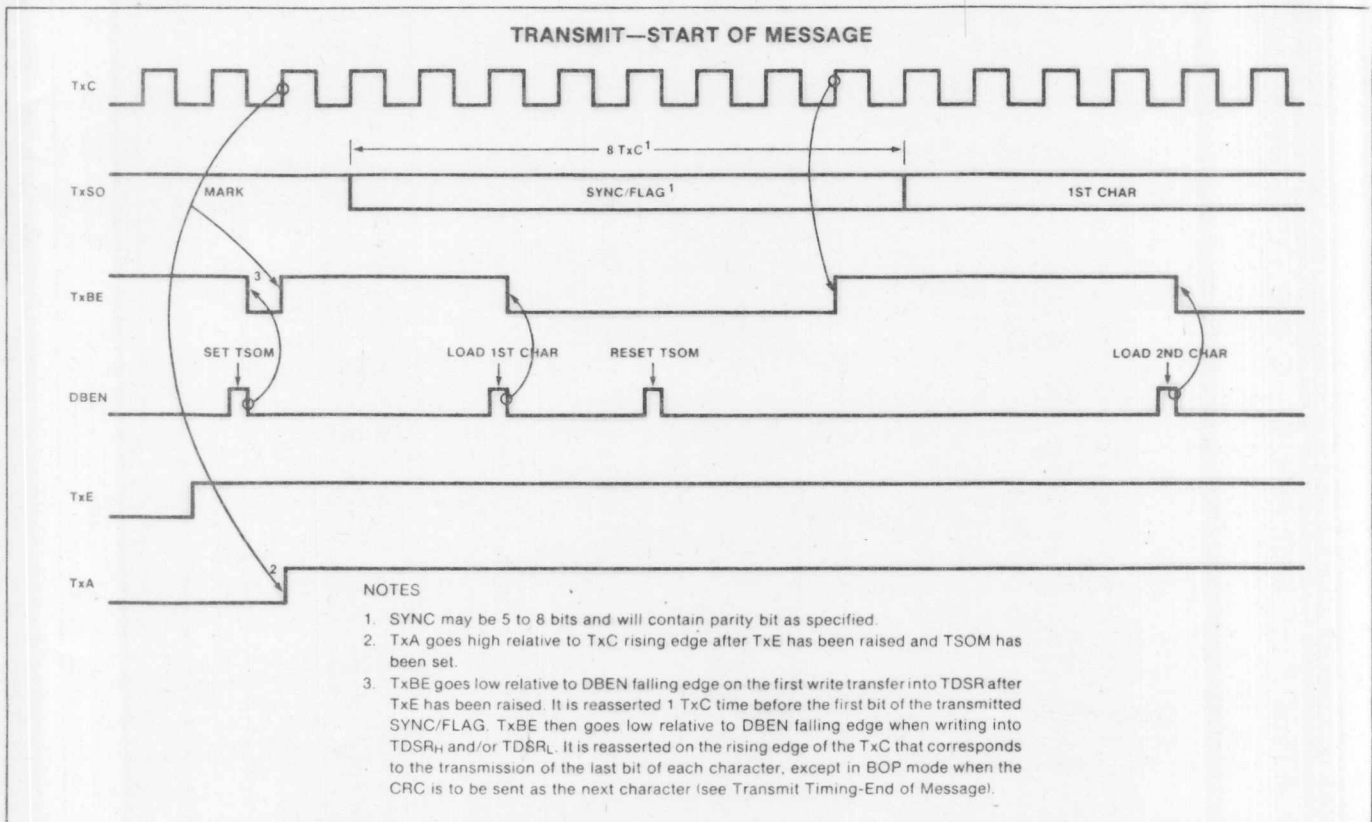
## PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design and process changes and improvements.

## TIMING DIAGRAMS

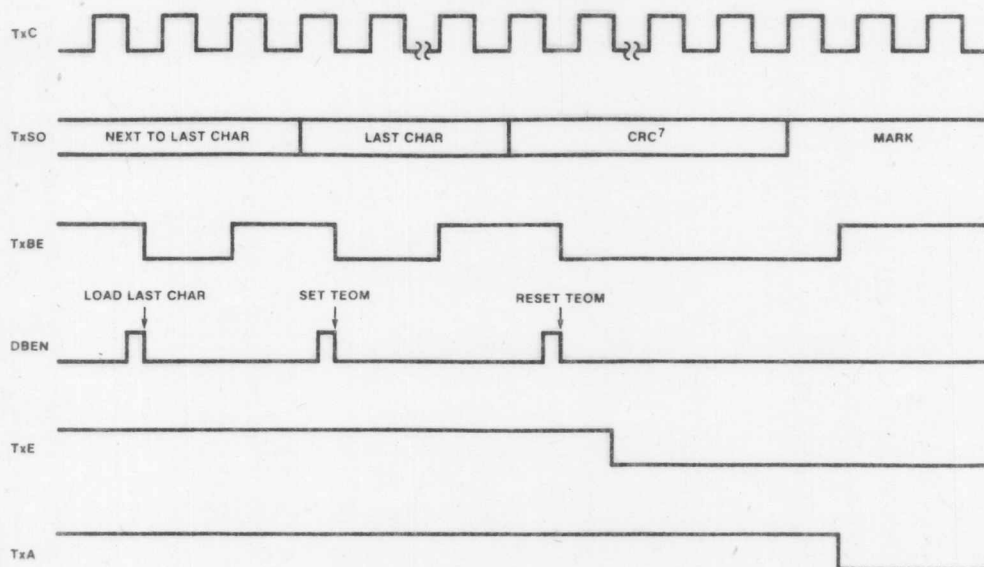


TIMING DIAGRAMS (Cont'd)



## TIMING DIAGRAMS (Cont'd)

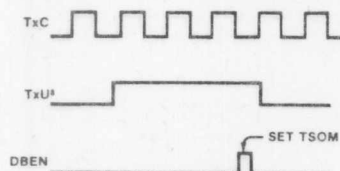
## TRANSMIT TIMING—END OF BCP MESSAGE



## NOTES

7. When 2652 generated CRC is not required, TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be dropped before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO.

## TRANSMIT UNDERRUN

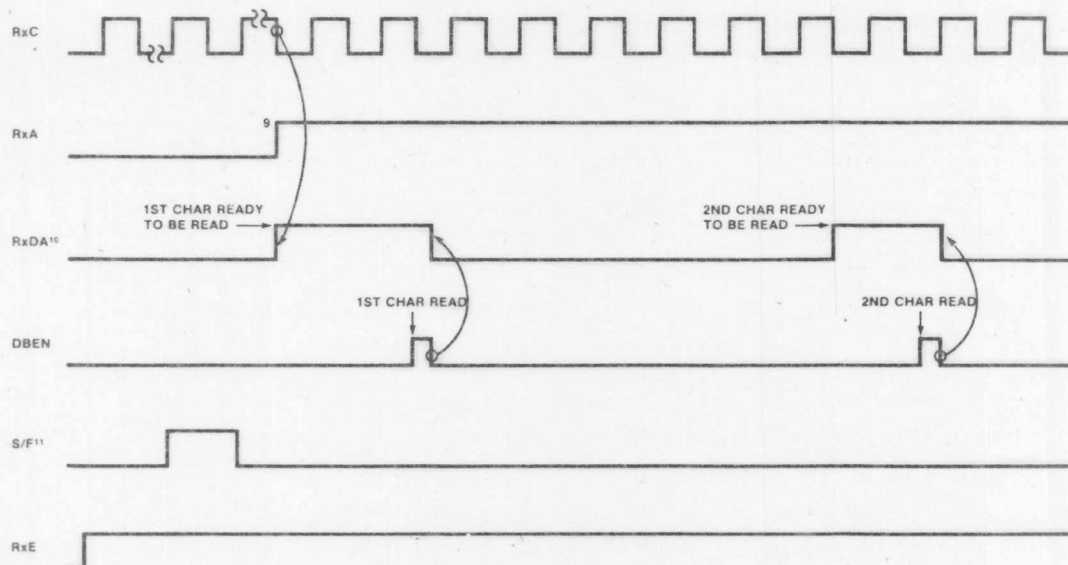


## NOTES

8. TxU goes active relative to TxC falling edge if TxBE has not been serviced after  $n-1/2$  TxC times (where  $n$  = transmit character length). TxU is reset on DBEN falling edge.

## TIMING DIAGRAMS (Cont'd)

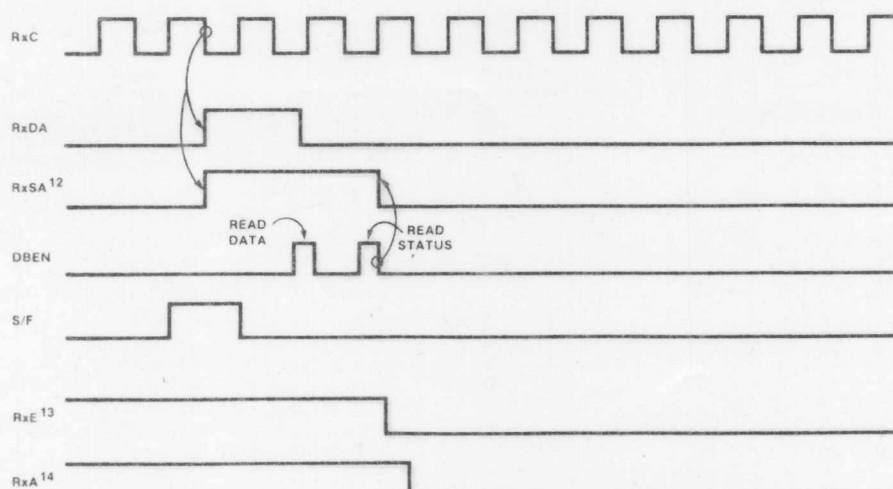
## RECEIVE—START OF MESSAGE



## NOTES

9. RxA goes high relative to falling edge of RxC when RxE is high and:
  - a. A data character following two SYNC's is in RxDB (BCP mode)
  - b. Character following FLAG is in RxDB (BOP primary station mode)
  - c. Character following FLAG is in RxDB and character matches the secondary station address or All Parties Address (BOP secondary station mode).
10. RxDA goes high on RxC falling edge when a character in RxDB is ready to be read. It comes up before RxSA and goes low on the falling edge of DBEN when RxDB is read.
11. S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

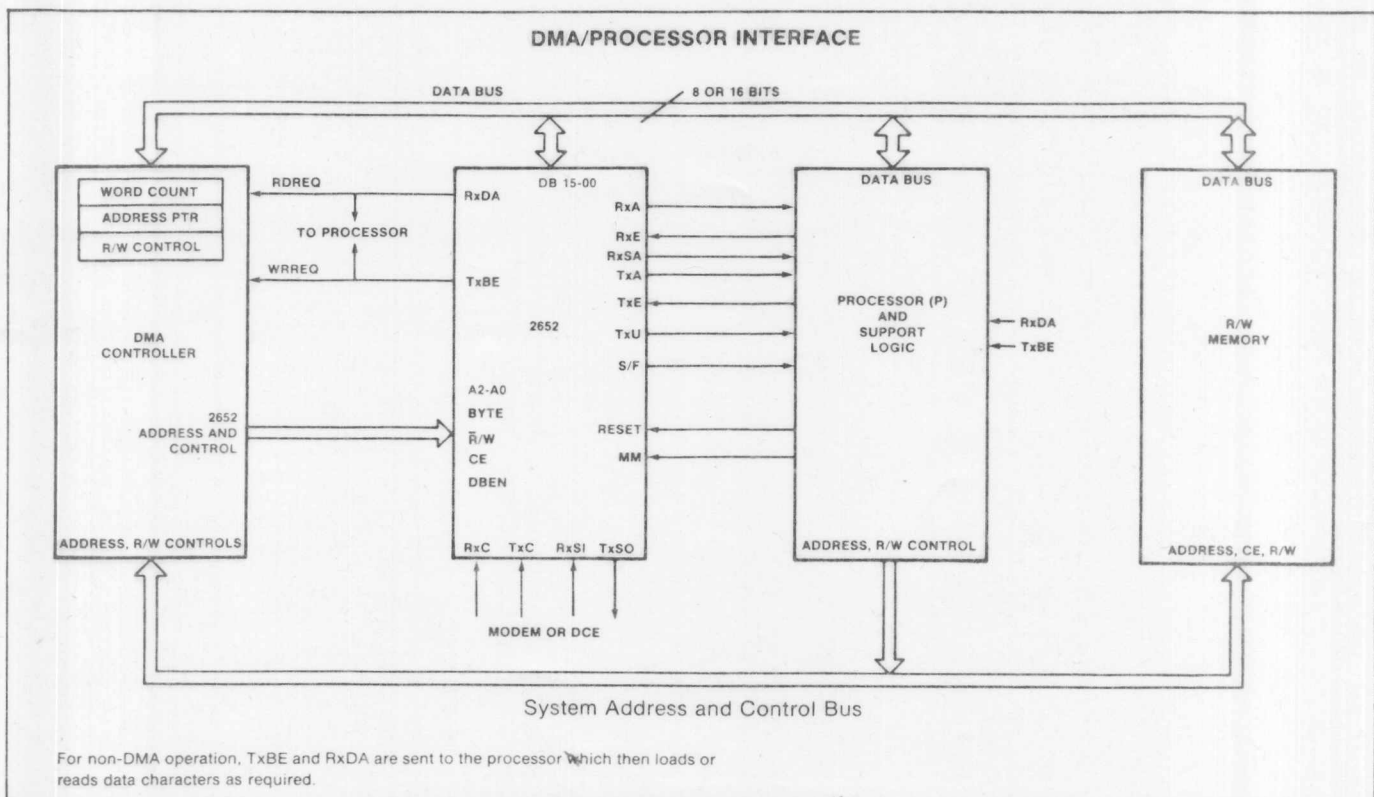
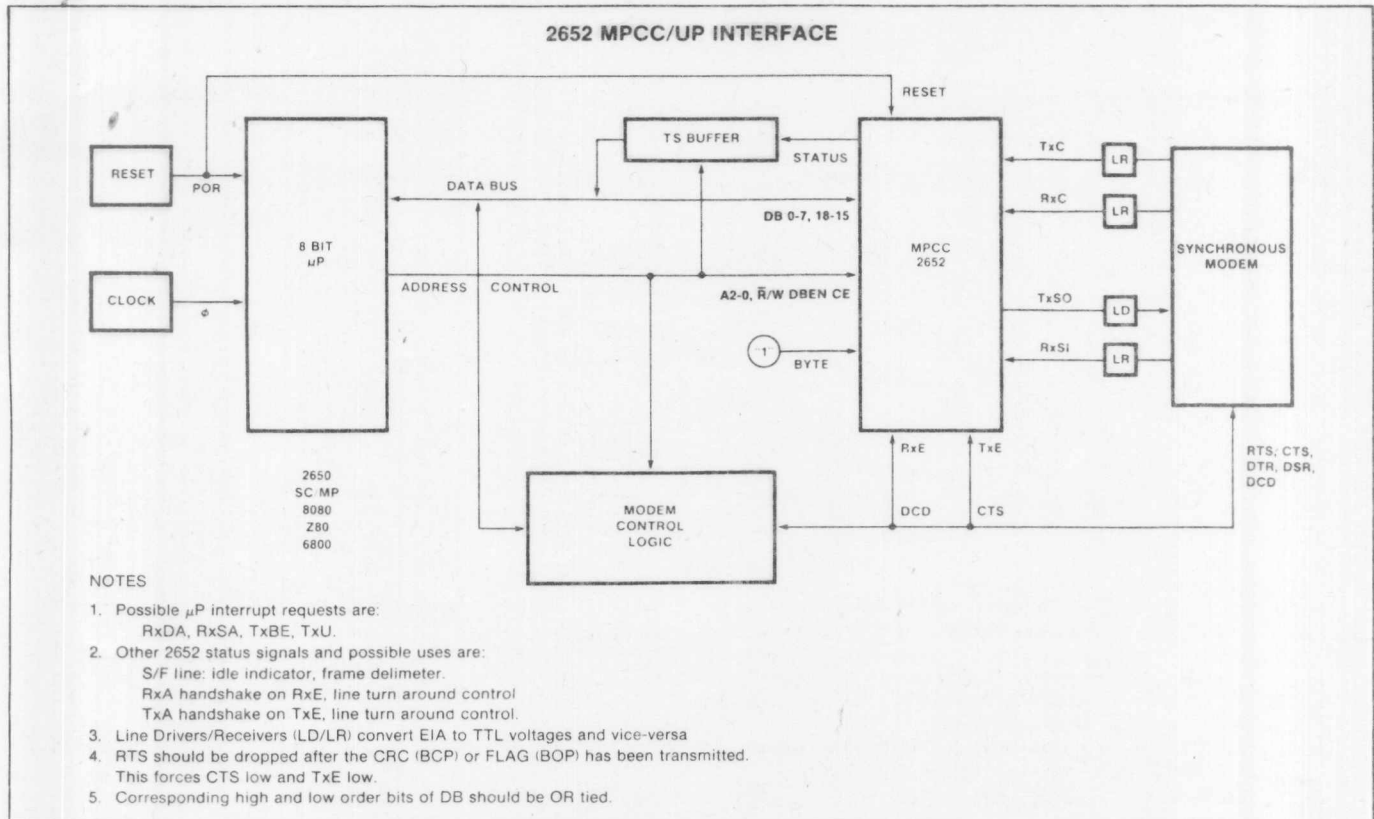
## RECEIVE END OF MESSAGE



## NOTES

12. At the end of a BOP message, RxSA goes high when FLAG detection ( $S/F = 1$ ) forces REOM to be set. Processor should read the last data character (RDSRL) and status (RDSRH) which resets RxDA and RxSA respectively. For BCP end of message, RxSA may not be set. The processor should read the last data character and the status.
13. RxE must be dropped for BCP but may be left on at the end of a BOP message (see BOP Receive Operation).
14. RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message; or when RxE is dropped.

## TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont'd)

